AS5016
16-Bit, 5-MSPS, SAR ADC with LVDS & SPI Interface

Product Preview(preliminary)

Features

• Sample Rate: 5 MSPS
• No Latency Output
• Excellent DC and AC Performance:
  - INL: ±0.5 LSB (Typ), ±1.5 LSB (Max)
  - DNL: ±0.75 LSB (Max), 18-Bit NMC
  - SNR: 100 dB
  - THD: –118 dB
• Wide Input Range:
  - Unipolar Differential Input Range: ±VREF
  - VREF Input Range: 2.5 V to 5 V, Independent of AVDD
• Low-Power Dissipation:
  - TBD mW at 5 MSPS (AVDD Only)
  - TBD mW at 5 MSPS (Total)
  - Flexible Low-Power Modes Enable Power Scaling with Throughput
• LVDS: Output data interface
• SPI: Enhanced Serial Interface
• Fully-Specified Over Industrial Temperature Range: –40°C to +85°C
• Small Footprint: 4-mm × 4-mm VQFN

Typical Applications

• Medical Imaging
• High-Precision, High-Speed Industrial
• Test and Measurement

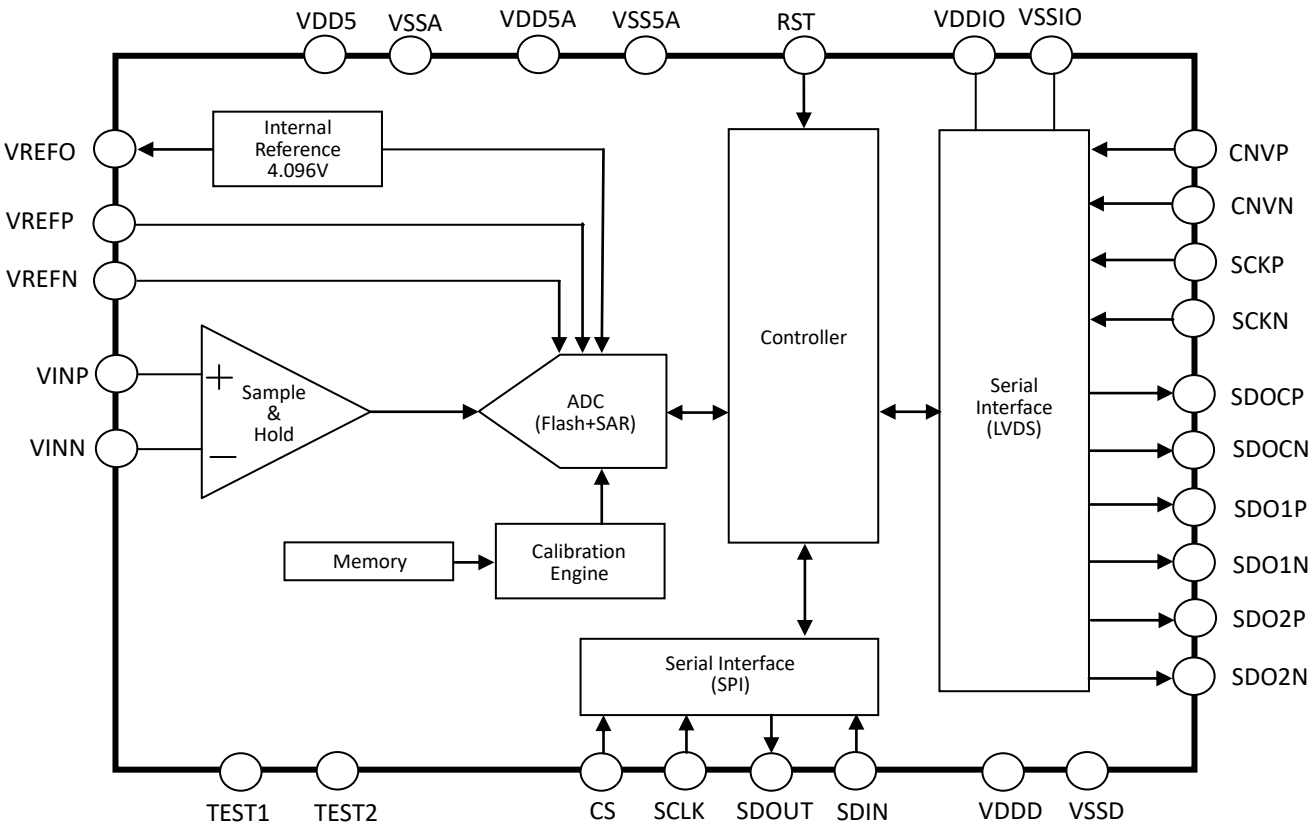
Overview

The AS5016 is a successive approximation register (SAR) type of AD converter IC, which can simultaneously convert analog signal to 18-bit data at 5Msps. This IC supports differential input of analog signals. The SPI interface is used for operation setting, and the LVDS interface is used for controlling AD-conversion and getting AD-data.

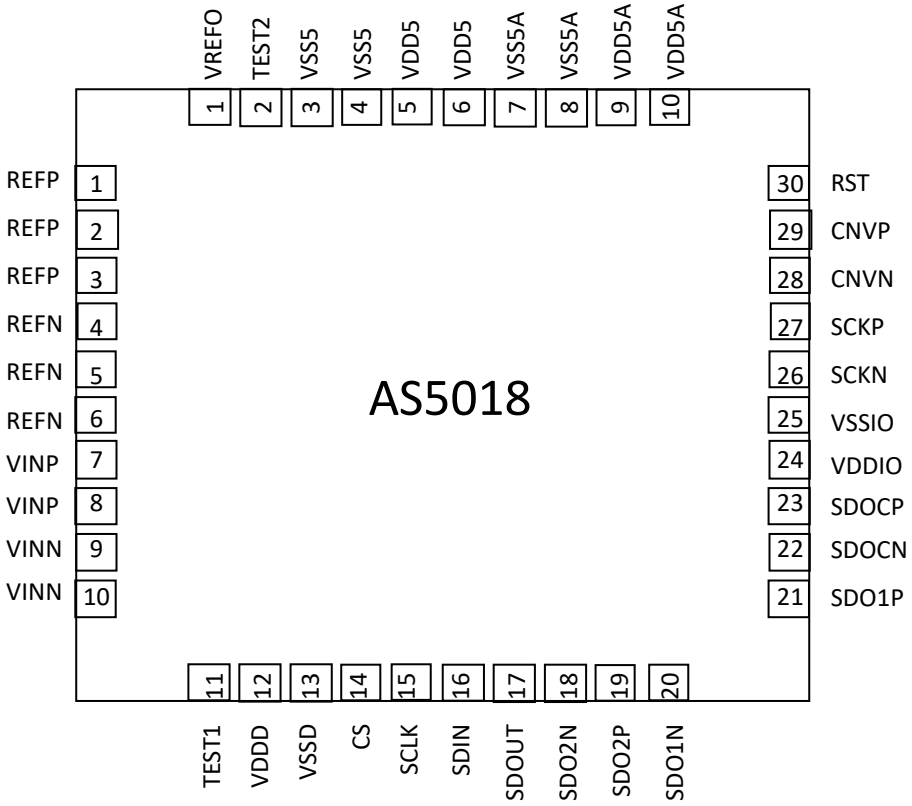
Functions

• 16-Bit 5Msps Successive Approximation Resister Type Analog to Digital Converter IC
• 16bit High Resolution
• 5Msps High Sampling Rate
• Differential Analog Input
• LVDS Outputs

Block Diagram



Pin Configuration



Terminal Explanations

PIN No.	Symbol	Type	Function
1~3	REFP	Input	VREF Positive Voltage Supply (VREF)
4~6	REFN	Input	VREF Negative Voltage Supply (VSS)
7~8	VINP	Input	Differential Positive Analog Input
9~10	VINN	Input	Differential Negative Analog Input
11	TEST1	I/O	Connect to VSS (For Outgoing Inspection)
12	VDDD	Power	1.8V Supply with a 10uF capacitor
13	VSSD	Power	The VSS for VDDD
14	CS	Input	Serial Interface for operation setting (Chip Select)
15	SCLK	Input	Serial interface for operation setting (Clock)
16	SDIN	Input	Serial interface for operation setting (Data-in)
17	SDOUT	Output	Serial interface for operation setting (Data-out)
18	SDO2N	Output	LVDS Negative Output 2
19	SDO2P	Output	LVDS Positive Output 2
20	SDO1N	Output	LVDS Negative Output 1
21	SDO1P	Output	LVDS Positive Output 1
22	SDOCN	Output	LVDS Clock Negative Output
23	SDOCP	Output	LVDS Clock Positive Output
24	VDDIO	Power	1.8V Supply with a 10uF capacitor
25	VSSIO	Power	The VSS for VDDD
26	SCKN	Input	LVDS Clock Negative Input
27	SCKP	Input	LVDS Clock Positive Input
28	CNVN	Input	LVDS Negative Input (For starting conversion)
29	CNVP	Input	LVDS Positive Input (For starting conversion)
30	RST	Input	ADC Setting Reset
31~32	VDD5A	Power	5V Supply with a 10uF capacitor
33~34	VSS5A	Power	The VSS for VDDD
35~36	VDD5	Power	5V Supply with a 10uF capacitor
37~38	VSS5	Power	The VSS for VDDD
39	TEST2	Output	Connect to nothing (For Outgoing Inspection)
40	VREFO	Output	Internal Reference Voltage Output 4.096V

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Supply Voltage 1	VDD5 VDD5A	-0.3	6.0	V
Supply Voltage 2	VDDD VDDIO	-0.3	2.1	V
VREFN voltage	VREFP	-0.3	VDD5+0.3	V
VREFN voltage	VREFN	-0.3	0.3	V
Analog input voltage	VINP VINN	GND-0.3	VDD5+0.3	V
Digital input voltage	(*1)	GND-0.3	VDDD+0.3	V
LVDS voltage	(*2)	GND-0.3	VDDIO+0.3	V
VREFO output current	Ivrefo	-	1	mA
Storage temperature	Tstg	-65	150	°C
Power dissipation (On board)	Pd	-	(TBD)	W

(*1) CS, SCLK, SDOUT, SDIN, RST

(*2) CNVP, CNVN, SCKP, SCKN, SDOCP, SDOCN, SDO1P, SDO1N, SDO2P, SDO2N

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Operating Ambient Temperature	Top	-40	-	125	°C
VDD5, VDD5A operating voltage	5Vop	4.75	5	5.25	V
VDDD, VDDIO operating voltage	1P8Vop	1.71	1.8	1.89	V

Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
Analog Supply Current	Iavop		-	40.0	TBD	mA
Digital supply current	I_{dv}	fsample=5Mpsps	-	TBD	-	mA
Analog Input						
Full-scale input range	FSR		-Vref	-	Vref	V
Absolute input voltage (+)	Vinp		-0.1	-	Vref+0.1	V
Absolute input voltage (-)	Vinn		-0.1	-	Vref+0.1	V
Common mode voltage	Vinc		Vref/2 -0.2	Vref/2	Vref/2 +0.2	V
Input capacitance	Cina		-	30	-	pF
Input leakage current	Iina		-	1.0	-	nA
Reference voltage Input						
Reference input voltage	Vref		3.900	4.096	4.150	V
Input Current	Iref		-	TBD		µA
Reference voltage (Internal)						
Reference input voltage	Vrefi		3.900	4.096	4.150	V
Source current	Irefi	Static Load	-	-	10	µA
Line Reguration	Lreg	VDD5=4.75V to 5.25V	-	1	-	mV
Reference voltage thermal drift	dVrefi/dT		-	5	-	ppm/°C
Resolution						
Resolution	Reso		-	-	18	Bits
No Missing codes			-	TBD	-	Bits
Sampling Dynamics						
Data rate	fsample		-	-	5	Msps
Aperture delay	tap		-	TBD	-	ns
Aperture jitter	tapj		-	TBD	-	ns

(*3) Specified by design

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DC accuracy						
Integral Nonlinearity	INL		-2	-	2	LSB (*6)
Differential nonlinearity	DNL		-1	-	2	LSB
Input offset voltage	Vof		-0.5	-	0.5	mV
Input offset thermal drift	dVof/dT		-	0.5	-	uV/°C
Gain error	Gerr		-0.10	-	0.10	%FS
Gain error thermal drift	dGerr/dT		-	1.0	-	ppm/°C
Common mode rejection ratio	CMRR		-	81	-	dB
AC accuracy						
Total harmonic distortion	THD	-0.5dB [full scale] at 10kHz input	-	-114	-	dB
		-0.5dB [full scale] at 100kHz input	-	-102	-	dB
		-0.5dB [full scale] at 500kHz input	-	-100	-	dB
Signal to (noise + distortion) ratio	SINAD	-0.5dB [full scale] at 10kHz input	-	100	-	dB
		-0.5dB [full scale] at 100kHz input	-	95	-	dB
		-0.5dB [full scale] at 500kHz input	-	94	-	dB
Signal to noise ratio	SNR	-0.5dB [full scale] at 10kHz input	-	102	-	dB
		-0.5dB [full scale] at 100kHz input	-	101	-	dB
		-0.5dB [full scale] at 500kHz input	-	100	-	dB
Spurious free dynamic range	SFDR	-0.5dB [full scale] at 10kHz input	-	116	-	dB
		-0.5dB [full scale] at 100kHz input	-	109		dB
		-0.5dB [full scale] at 500kHz input	-	106	-	dB

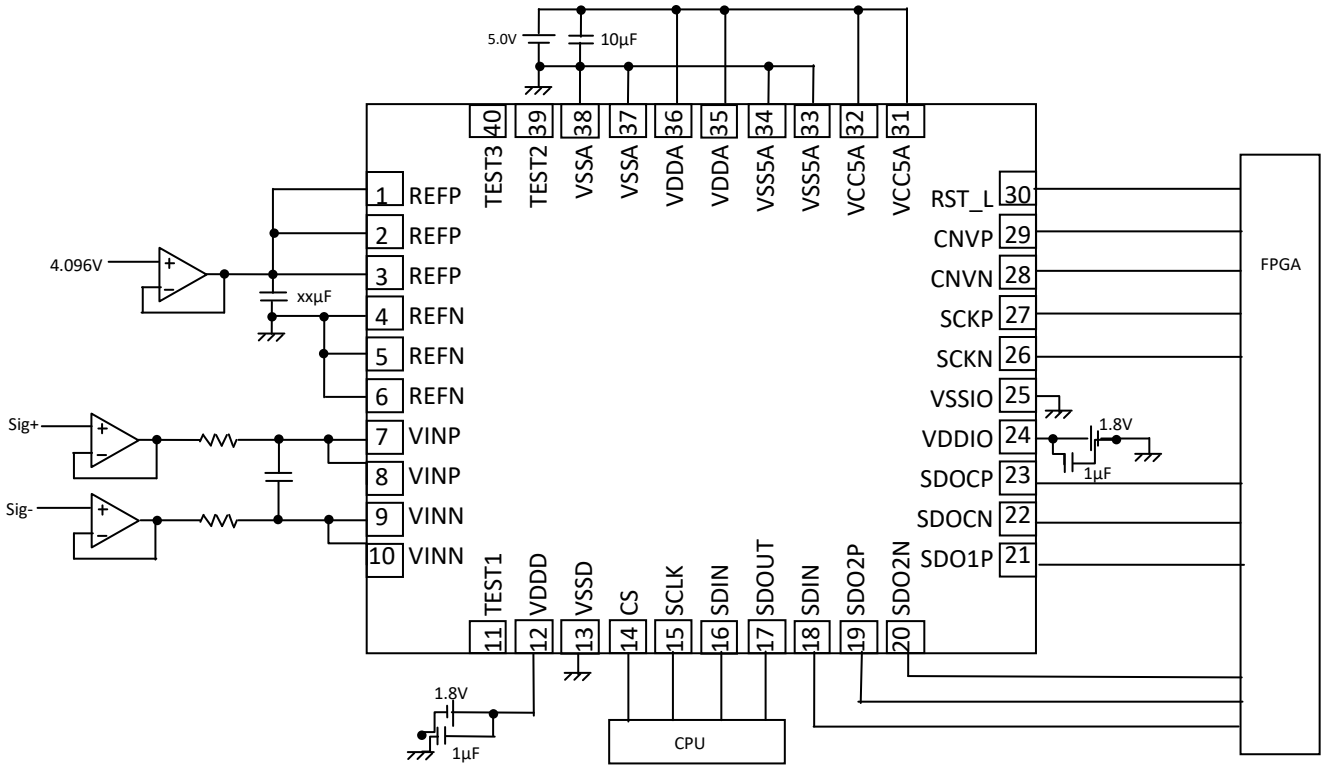
Small Signal bandwidth	BW_{FP}	-3dB	-	30	-	
Maximum input frequency	Finmax		2.50	-	-	

(*4) Specified by design

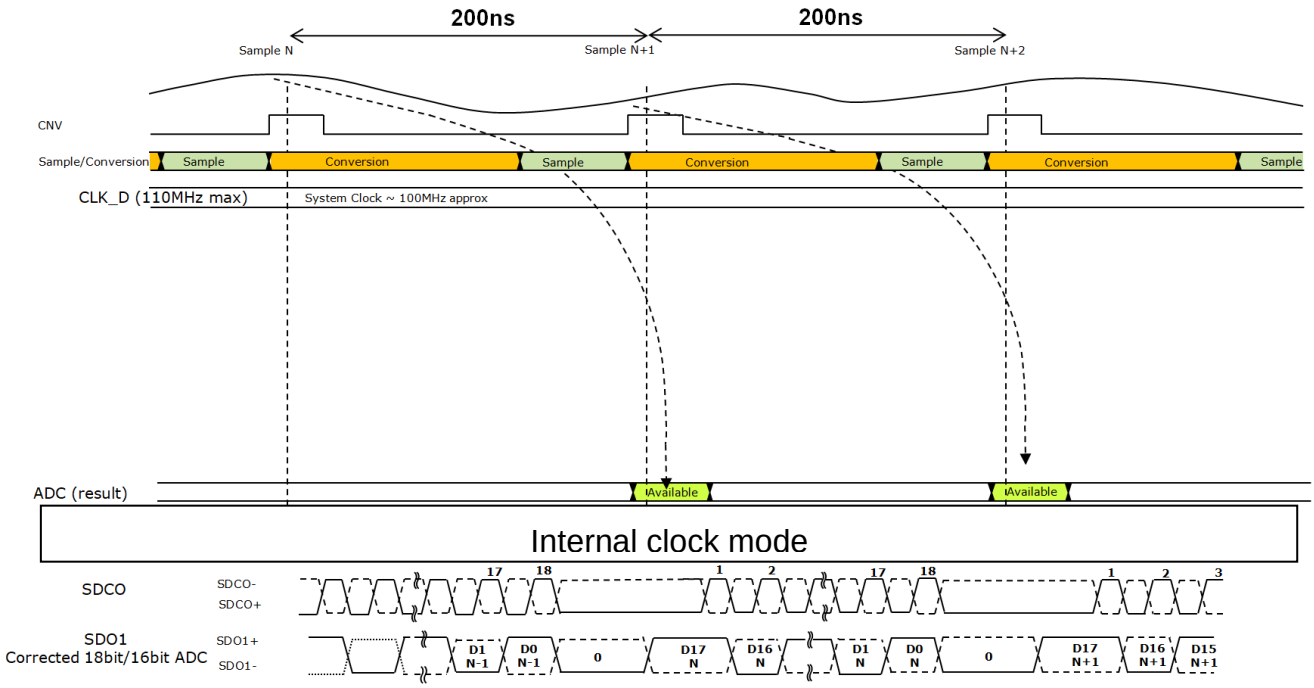
Timing Characteristics

Ta=-40℃～125℃, VDDA=VDD5A=5V, DVDD=VDDIO=1.8V, VREF=4.096、Sampling rate=5Msps

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SPI Interface						
Clock Frequency	f_{SCLK}		-	-	1	MHz
Clock duty	Duty		TBD	TBD	TBD	%
SPI input (CS, SCLK, SDIN)						
High level input voltage	Vih		0.7x DVDD	-	DVDD +0.3	V
Low level input voltage	Vil1	DVDD≧2V	-0.30	-	0.3x DVDD	V
SPI output (SDOUT)						
High level output voltage	Voh	Ioh=500μA source	0.8x DVDD	-	DVDD	V
Low level output voltage	Vol	Iol=500μA sink	0	-	0.2x DVDD	V
LVDS Interface						
Clock frequency	f_{SCK}		-	-	300	MHz
CNV High time	t_{CNH}		TBD	-	-	ns
Conversion time	t_{CONV}		-	TBD	-	ns
Acquisition time	t_{ACQ}		TBD	-	-	ns
Differential input voltage			175	350	650	mV
Common mode output voltage			0.800	1.250	1.700	V
Differential output voltage			175	350	650	mV
Common mode output voltage			1.125	1.250	1.375	V

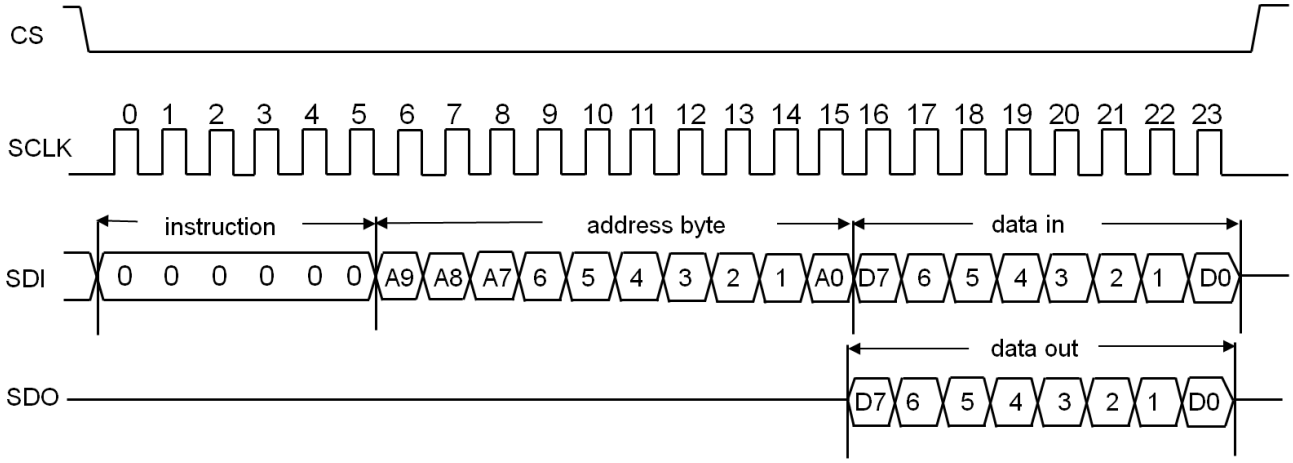

5.0V
10µF
40 TEST3
39 TEST2
38 VSSA
37 VSSA
36 VDDA
35 VDDA
34 VSS5A
33 VSS5A
32 VCC5A
31 VCC5A
1 REFP
2 REFP
3 REFP
4 REFN
5 REFN
6 REFN
7 VINP
8 VINP
9 VINN
10 VINN
30 RST_L
29 CNVP
28 CNVN
27 SCKP
26 SCKN
25 VSSIO
24 VDDIO
23 SDOCP
22 SDOCN
21 SDO1P
11 TEST1
12 VDDD
13 VSSD
14 CS
15 SCLK
16 SDIN
17 SDOUT
18 SDIN
19 SDO2P
20 SDO2N
4.096V
xxµF
Sig+
Sig-
1.8V
1µF
1.8V
1µF
CPU
FPGA

Analog Input and LVDS Output Timing Information



SPI Protocol and Timing Information

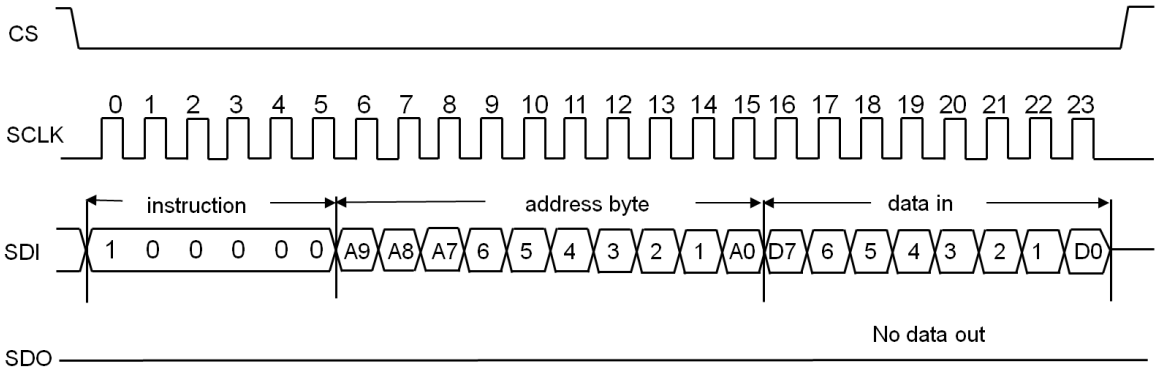
- SPI Interface Format & Protocol: 24bits
- Instruction: 6bits, Address: 10bits, Data: 8bits
- SCLK speed: 1MHz max



SPI format:

- Register write: 100000<A9A8>_<A7..0>_<DIN7..0>
- Register read: 100001<A9A8>_<A7..0>_00000000
- OTP write: 100010<A9A8>_<A7..0>_<DIN7..0>
- OTP read: 100011<A9A8>_<A7..0>_00000000
- OTP PPROG signal assert/deassert: (TBD)
- POR copy process status query: TBD
- No operation: 00000000_00000000_00000000

- Example: SPI register write



- Example: SPI register read